

**B.E. 7th Semester (CSE) Examination, December-2013**

**ADVANCED COMPUTER ARCHITECTURE**

**Paper-CSE-401 E**

*Time allowed : 3 hours] [Maximum marks : 100*

**Note : Attempt any five questions.**

1. (a) Differentiate between hardwired control and micro programmed control. 8  
(b) Describe virtual to real address translation mechanism. 12
2. (a) Assume a wafer has diameter of 0.20 m and costs 10000 for a particular production run. Compute the cost per die for die area =  $2.5\text{cm}^2$  and for  $0.015\text{ m}^2$  if defect density = 0.9 defects/ $\text{cm}^2$ . 14  
(b) What is cycle quantization ? Find the effect of cycle quantization on pipelining. 6
3. (a) Explain set associative mapping in detail. 10  
(b) Explain principle of logical inclusion in cache memory. 10
4. Explain Hellerman, Strecker and Rau's model in memory system design. 20

5. (a) Compare vector and multiple issue processor. 10  
(b) Explain synchronization and memory coherency in shared memory multiprocessors. 10
6. Write a program in L/S, R/M architecture for addition of all the elements of an array. 20
7. (a) Explain various cache write policies. 10  
(b) Explain various functional units of vector processor. 10
8. Write notes on :  
(a) Pipelining  
(b) Portioning in shared memory multiprocessor.  
(c) Flores memory model. 20